





# ARM


## SESSION 2



### Topics Covered

- ARM Architecture
- ARM Registers
- Processing Modes
- Interrupts
- Pipeline


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### Overview of ARM7

- **32-bit RISC processor** (32-bit data & address bus)
- **Big and Little Endian operating modes**
- **High performance RISC**  
(17 MIPS sustained @ 25 MHz (25 MIPS peak) @ 3V)
- **Low power consumption**  
(0.6mA/MHz @ 3V fabricated in .8µm CMOS)
- **Fully static operation**  
(ideal for power-sensitive applications)
- **Fast interrupt response**  
(for real-time applications)
- **Virtual Memory System Support**
- **Excellent high-level language support**
- **Simple but powerful instruction set**



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### ARM7 Applications

- **The ARM7 is ideally suited to those applications requiring RISC performance from a compact, power-efficient processor**
  - **Telecomms - GSM terminal controller**
  - **Datcomms - Protocol conversion**
  - **Portable Computing - Palmtop computer**
  - **Portable Instrument - Handheld data acquisition unit**
  - **Automotive - Engine management unit**
  - **Information systems - Smart cards**
  - **Imaging - JPEG controller**

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# ARM Architecture

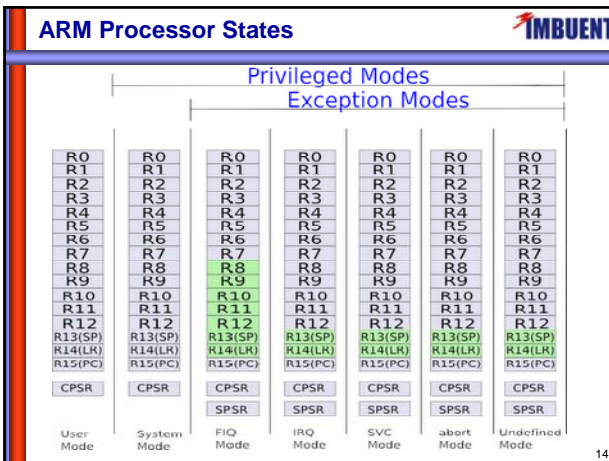


### ARM Architecture Overview

- Data items are placed in register file
- Data operations can be performed only on data in the register
- Barrel shifter on data path can be used to shift the data before processing
- Increment or decrement operation can also be performed on data

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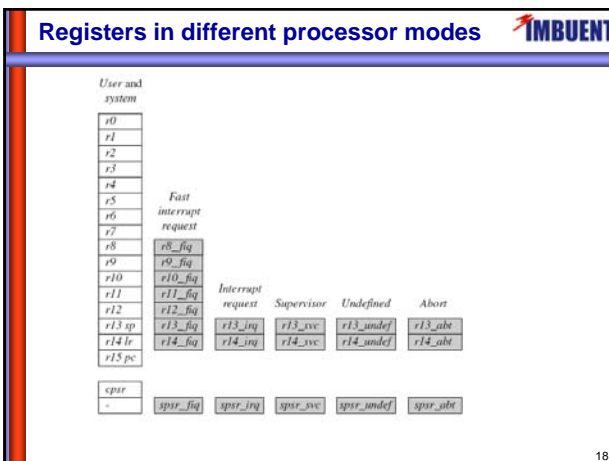
- ### Processor States
- The ARM has seven operating modes:
    - User** (unprivileged mode under which most tasks run)
    - FIQ** (entered when a high priority (fast) interrupt is raised)
    - IRQ** (entered when a low priority (normal) interrupt is raised)
    - Supervisor** (entered on reset and when a Software Interrupt instruction is executed)
    - Abort** (used to handle memory access violations)
    - Undef** (used to handle undefined instructions)
    - System** (privileged mode using the same registers as user mode)
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### Mode Bits of CPSR register

Mode	Abbreviation	Privileged	Mode[4:0]
Abort	abt	yes	10111
Fast interrupt request	fiq	yes	10001
Interrupt request	irq	yes	10010
Supervisor	svc	yes	10011
System	sys	yes	11111
Undefined	und	yes	11011
User	usr	no	10000

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- ### Privileged mode
- Privileged mode**
    - user has full access to CPSR register
  - User mode**
    - full access only to condition flags
    - rest of flags are read only
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- ### Privileged mode
- Except system mode all modes have different copy of registers
  - These copies can be accessed by adding mode name in register
  - In FIQ mode banked registers are r8\_fiq to r14\_fiq
  - In rest of mode r13 and r14 register get refreshed copy
  - Register name in instruction will be same
    - Ex MOV R0,R13 is same in usr and fiq mode
    - But register R13 in fiq mode is R13\_fiq
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### Changing mode

- Mode can be changed by writing directly in mode bits of CPSR register
- Mode change by interrupts and exceptions
  - Fiq => **FIQ Mode**
  - Irq => **IRQ Mode**
  - Reset => **Supervisor Mode**
  - Software Interrupt => **Supervisor Mode**
  - Data abort => **Abort Mode**
  - Prefetch abort => **Abort Mode**
  - Undefined instruction => **Undefined Mode**

### Register Mode: Changing from user mode to fiq mode

### Instruction set

- ARM Mode
  - Instruction size is 32 bit
  - Total instructions are 58
  - All instructions can have conditional execution
  - Data instructions has access to barrel shifter
  - CPSR can be accessed fully in privileged mode
- Thumb Mode
  - Instruction size is 16 bits
  - Total core instructions are 30
  - Conditional execution is only in branch instruction
  - No direct access to CPSR

### Pipeline

- Pipeline mechanism is used to make execution of instructions fast
- Next instruction is fetched while previous instructions are decoding and executing

### 3-Stage Pipeline

- ARM7 has three stage pipeline

**Fetch:** Reading instruction from memory  
**Decode:** identify instruction to be executed  
**Execute:** processing the instruction and storing the result in memory

- Each instruction take only one cycle to complete after pipeline is filled

### 5-Stage Pipeline

- ARM9 has five stage pipeline

**Fetch:** Reading instruction from memory  
**Decode:** identify instruction to be executed  
**Execute:** processing the instruction and storing the result in memory  
**Memory:**  
**Write:**

- Achieve 1.1Dhrystone MIPS per sec

### Pipeline Characteristics

- Execution of first instruction take place only after 3 cycles

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### Pipeline Characteristics

- value of PC is PC + 8 after execution of current instruction

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### Exceptions and Interrupts

Exception/interrupt	Shorthand	Address
Reset	RESET	0x00000000
Undefined instruction	UNDEF	0x00000004
Software interrupt	SWI	0x00000008
Prefetch abort	PABT	0x0000000c
Data abort	DABT	0x00000010
Reserved	—	0x00000014
Interrupt request	IRQ	0x00000018
Fast interrupt request	FIQ	0x0000001c

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- ### Memory Management
- Two type of memory management
- **MPU: Memory Protection Unit**
    - > Limited number of memory regions
    - > Each region is controlled by special coprocessor registers
    - > Each region is defined as specific set of permission
    - > used when system require memory protection but do not have complex memory map
  - **MMU: Memory Management Unit**
    - > Unlimited number of memory regions
    - > Each region has virtual memory
    - > VM to PM conversion is done by memory address translation table
    - > Memory access rights are also given in translation table
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- ### Coprocessor
- used to enhance processing capabilities of processor
  - Coprocessor can execute extended instructions
  - coprocessor is fully configurable
  - ARM has dedicated instruction to access coprocessor
  - Example **VFP** Vector Floating Point operations
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